

A Novel and Simple Single-Phase Modulator for the Nested Neutral-Point Clamped (NNPC) Converter

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Abstract—The nested neutral-point clamped (NNPC) converter is a four-level converter topology for medium-voltage applications with interesting properties such as operating over a wide range of voltages (2.4–7.2 kV) without the need for connecting the power semiconductor in series, high quality output voltage, and less number of components in compare to other classical four-level topologies. The control and balance of the flying capacitors (FCs) of the NNPC converter can be done by different control techniques taking advantage of the large number of redundant switching states. This paper presents a simple single-phase modulator for the NNPC converter, which can be applied to each phase of a three-phase NNPC converter. The proposed simple technique can control and balance the FCs to their desired values. Performance of the proposed technique under different operating conditions is investigated in the MATLAB/Simulink environment. The feasibility of the proposed converter is evaluated experimentally.

Index Terms—DC–AC power conversion, multilevel converter, sinusoidal pulse width modulation (SPWM).

I. INTRODUCTION

Multilevel converters are a very attractive solution for medium-voltage high-power conversion applications; such as motor drives, microgrids, and distributed generation systems. The main features of these topologies, as compared with the two-level voltage-source converters (VSC), are their capabilities to reduce: 1) harmonic distortion of the ac-side waveforms; 2) dv/dt switching stresses; 3) switching losses; and 4) minimize or even eliminate the interface transformer [1].

Many multilevel topologies have been developed, among them, the neutral-point clamped (NPC), flying capacitor (FC), and the cascaded H-bridge (CHB), are the most studied and well-established multilevel topologies, which are so-called classic multilevel topologies [1]–[5]. Although the classic multilevel converters have been commercialized by major manufacturers, they have some drawbacks, which limit their applications. For instance, an NPC structure with higher number of levels is less attractive and this is because the number of clamping diodes

increases substantially with the voltage level. For FC structure, the number of FCs increases with the voltage level. The CHB topology needs a large number of isolated dc sources and an expensive and bulky phase-shifting transformer.

Numbers of variants and new multilevel converters have been proposed in literatures [6]–[15]; however, most of them are variations to the three classic multilevel topologies or hybrids between them, which are so-called advanced multilevel topologies. Among the recent topologies, the following topologies have found practical application, which are commercialized by manufacturers; the five-level H-bridge NPC (5L-HNPC) [6]–[9], the three-level active NPC (3L-ANPC) [10]–[11], the five-level active NPC (5L-ANPC) [12]–[15], and the four-level nested neutral-point clamped (NNPC) converter [16].

A 5L-HNPC is the H-bridge connection of two classic 3L-NPC phase legs, which makes a five-level converter. This topology like an H-bridge topology requires isolated dc sources with the phase-shifting transformer, which increases the cost and complexity of the converter.

A 3L-ANPC is an improved three-level NPC, which can control the loss distribution among the switches of the converter. This topology has higher number of the devices as compared to three-level NPC with the same number of output voltage levels. This increases the cost and complexity of the overall converter.

A 5L-ANPC is a combination of a 3L-ANPC and 3L-FC. The main drawback of the 5L-ANPC converter is that the voltage rating of the switches in one phase of the converter are different. The voltage rate of the outer switches are half of the dc-bus voltage and the voltage rate of the inner switches are $1/4$ of the dc-bus voltage.

The NNPC converter, as shown in Fig. 1, is a recent multilevel converter topology with interesting properties such as [16]:

- 1) it can operate for a wide range of 2.4–7.2 kV without device in series;
- 2) it has fewer parts, in compare to same rate previous multilevel converters;
- 3) all the switches have the same voltage stress and equal to one third of the input voltage;
- 4) it does not need any complex transformer;
- 5) the NNPC converter mitigates some drawbacks of the existing topologies, however still the voltage rate that this converter can operate without connecting power semiconductor devices in series is limited to 7.2 kV.

One of the main common issues for the multilevel converter is to control the capacitor voltages at their nominal values to

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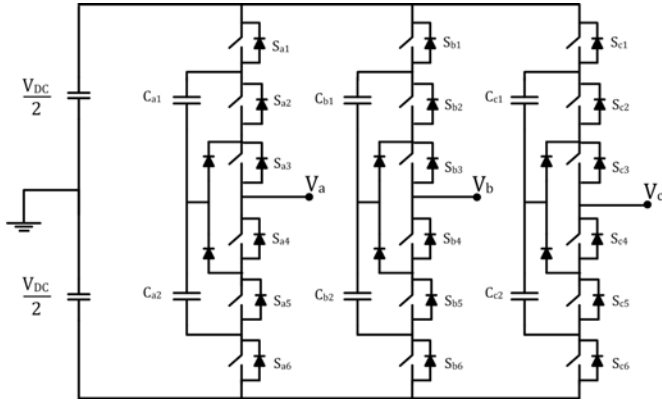


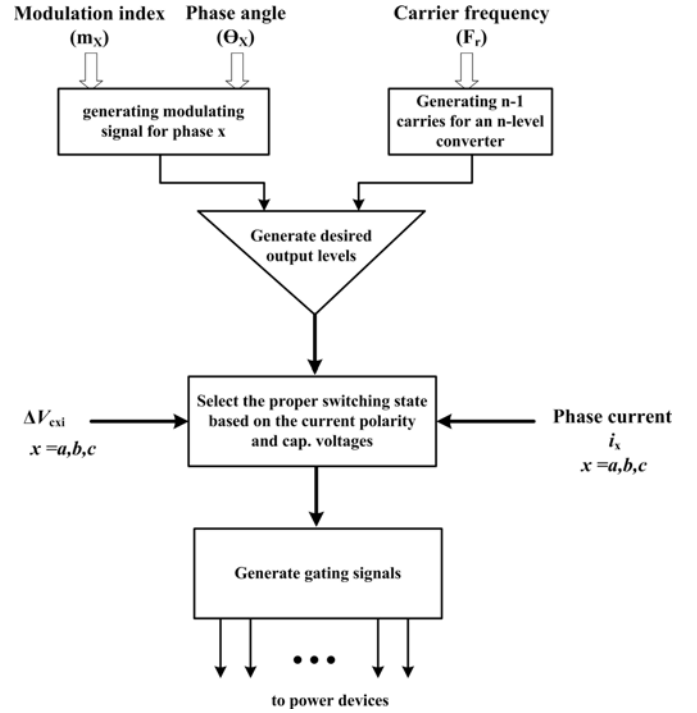
Fig. 1. Proposed NNPC converter.

operate the converter properly. For example, for a diode-clamped converter the dc-link capacitor voltages should be balanced at nominal values and for a FC converter the voltages of the FCs should be regulated. Different strategies can be applied to control the voltage of capacitors in multilevel converters. One approach is to use auxiliary converter to perform the voltage balancing, which increases the cost and complexity of the overall converter particularly at high-voltage/power levels [17]–[21].

Various modulation strategies have been developed and studied for multilevel converter topologies [22]–[33]. Since the multilevel converters are intended to be used in high-power applications; there are two major challenges in the selection of modulation strategies; high power quality and minimum switching frequency. One modulation strategy for high-power multilevel converters is space vector modulation (SVM), which offers flexibility in the selection of best switching state among the redundant switching states to enhance the dc-bus voltage utilization and better harmonic performance.

The SVM scheme generates all the available switching states, switching sequences, and calculates the duty cycles. Some papers just propose new approaches to generate switching states for multilevel converters and they do not address the control issue of the capacitor voltages such as [22], [23] and [34]. Some papers such as [31], [32], and [35], address the issue of voltage balancing of the capacitors using minimum energy property. In this approach, based on the defined cost function, which tries to minimize the difference between the nominal voltage value and the actual value, the best switching states among the all possible switching states can be selected, and finally, apply to the converter. The SVM strategy can generate redundant switching states, particularly at lower modulation index. Moreover, depends on the converter topology, there may exist some redundant switching states for each voltage level. These redundancies increase the number of calculations in the cost function in order to select the best switching state [5], [16], [32]. By the increase in the number of levels, the computational burden for the real-time implementation will increase and sometimes the real-time system cannot handle this task properly, which deteriorate the performance of the converter.

Another modulation scheme that is the most popular modulation scheme in industrial applications is sinusoidal PWM

Fig. 2. Block diagram of the proposed SPWM approach for phase x .

(SPWM). This modulation scheme is based on the multicarrier PWM strategy. The performance of the different SPWM strategies are studied analytically in [23] to show which SPWM strategy has the better harmonic performance. Moreover, the comprehensive comparison of the SPWM and SVM modulation schemes has been studied in [34].

The main focus of this paper is to propose a new approach using multicarrier SPWM strategy to generate multilevel output voltage, while regulating the voltage of capacitors. This approach employs the deviation of the capacitor voltages from their nominal values and based on the converter output current select the best switching state from the available redundant switching states to charge or discharge the capacitors, and finally, regulate the voltages of capacitors. This approach, unlike the SVM strategy, does not need any cost function and is very intuitive and simple to implement, however, it is very effective.

Fig. 2 shows the procedure of the proposed approach. In this procedure, first, the modulating signal for phase x ($x = a, b, c$) is compared to carriers ($n-1$ carriers for an n -level converter), and then, the desired output levels are determined.

Based on the desired output level, the corresponding switching state that generates this voltage level can be applied to the power switches. Moreover, there are some redundant switching states for some levels that come from the topology of the converter. For example, for a four-level FC converter, [32], there are three redundant switching states to generate the two middle levels and for a seven-level topology given in [5], there are more than three redundant switching states for each voltage level. Each redundant switching state is able to charge or discharge the capacitor based on the phase current. If the capacitor voltage is greater than the nominal value ($\Delta V_{xi} = V_{xi} - V_n > 0$), the

TABLE I
SWITCHING STATES OF THE FOUR-LEVEL NNPC AND CONTRIBUTION OF THE AC-SIDE CURRENTS TO THE FC VOLTAGES

State	Sx1	Sx2	Sx3	Sx4	Sx5	Sx6	VCx1	VCx2	Output Level
D	1	1	1	0	0	0	No Impact	No Impact	3
C2	1	0	1	1	0	0	Charging ($i_x > 0$)Discharging ($i_x < 0$)	No Impact	2
C1	0	1	1	0	0	1	Discharging ($i_x > 0$)Charging ($i_x < 0$)	Discharging ($i_x > 0$)Charging ($i_x < 0$)	
B2	1	0	0	1	1	0	Charging ($i_x > 0$)Discharging ($i_x < 0$)	Charging ($i_x > 0$)Discharging ($i_x < 0$)	1
B1	0	0	1	1	0	1	No Impact	Discharging ($i_x > 0$)Charging ($i_x < 0$)	
A	0	0	0	1	1	1	No Impact	No Impact	0

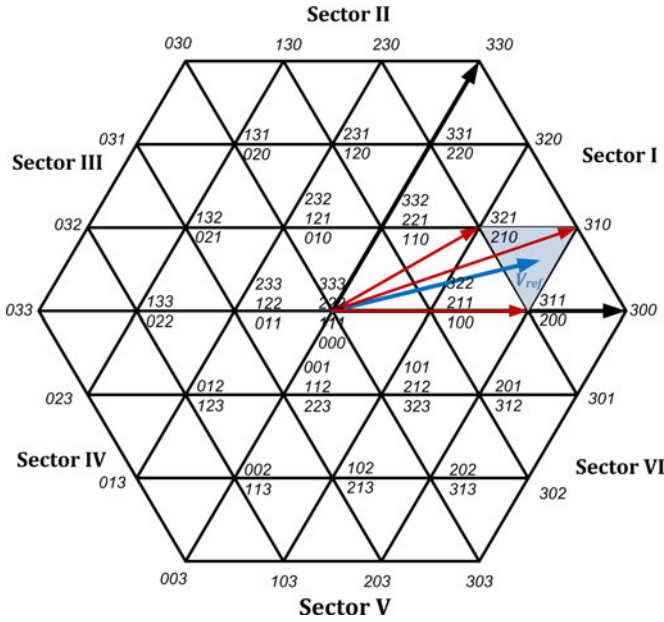


Fig. 3. Space vector diagram of a four-level converter.

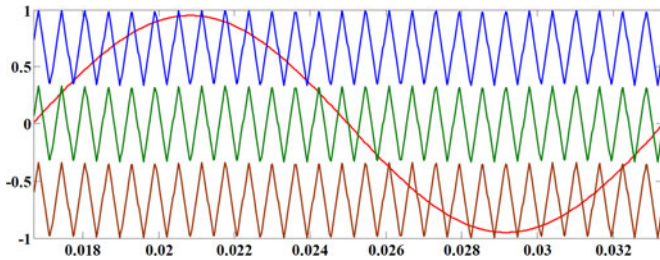


Fig. 4. Level-shifted multicarrier modulation for the NNPC inverter.

capacitor should be discharged and when the $\Delta V_{xi} < 0$ should be charged. Therefore, the appropriate switching state that can charge or discharge the capacitor can be selected and applied to the converter.

One of the main advantage of the proposed strategy is that, unlike the SVM strategy, this strategy can be applied for each phase of the converter separately, as a result when the converter is employed to be in different configurations such as the back-to-back structure, cascades H-bridge structure, and modular multilevel structure, the proposed modulation scheme can be implemented easily to generate the output multilevel voltage and also regulate the capacitor voltages. In this paper, this strategy is developed for an NNPC converter.

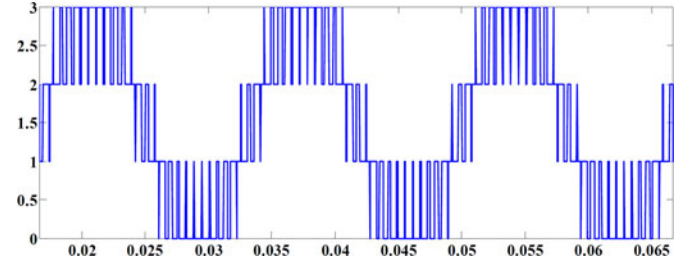


Fig. 5. Desired output levels based on modulating signal.

The proposed technique for the NNPC converter has the following features:

- 1) it can regulate the FC voltages at the desired values;
- 2) the implementation is very simple and can be generalized for different combination of the NNPC converter such as CHB-NNPC and MMC-NNPC.

This paper has the following structure; in Section II, the operation of the NNPC converter with an SVM technique will be explained briefly. Section III proposes a new and simple single-phase SPWM technique to control and balance the FC voltages for the NNPC converter. In Section IV, performance of the proposed technique under different operating conditions is investigated in the MATLAB/Simulink environment. The experimental results are presented in Section V.

II. NNPC CONVERTER WITH SVM TECHNIQUE

A. Operation of the NNPC Converter

The NNPC converter is a combination of a FC topology with NPC topology, which provides four level at the output voltage. The capacitor Cx_1 and Cx_2 , $x = a, b, c$ are charged to one third of the total dc-link voltage to ensure equally spaced steps in the output voltages. The NNPC converter in compare to the classic four-level topologies has less number of components and complexity. In compare to a four-level NPC converter, the number of diodes has been reduced from 18 to 6. In compare to a four-level FC converter, the number of FCs has been reduced from 9 to 6. Also, unlike the CHB converter, the NNPC converter does not need to have any isolated dc sources or phase-shifting transformers.

The list of switching combinations is shown in Table I. Four different output levels are achieved from six distinct switching combinations. The NNPC converter can take the advantage of redundancy in switching states to regulate the voltages of the FCs. As can be seen in Table I, for generating medium-voltage

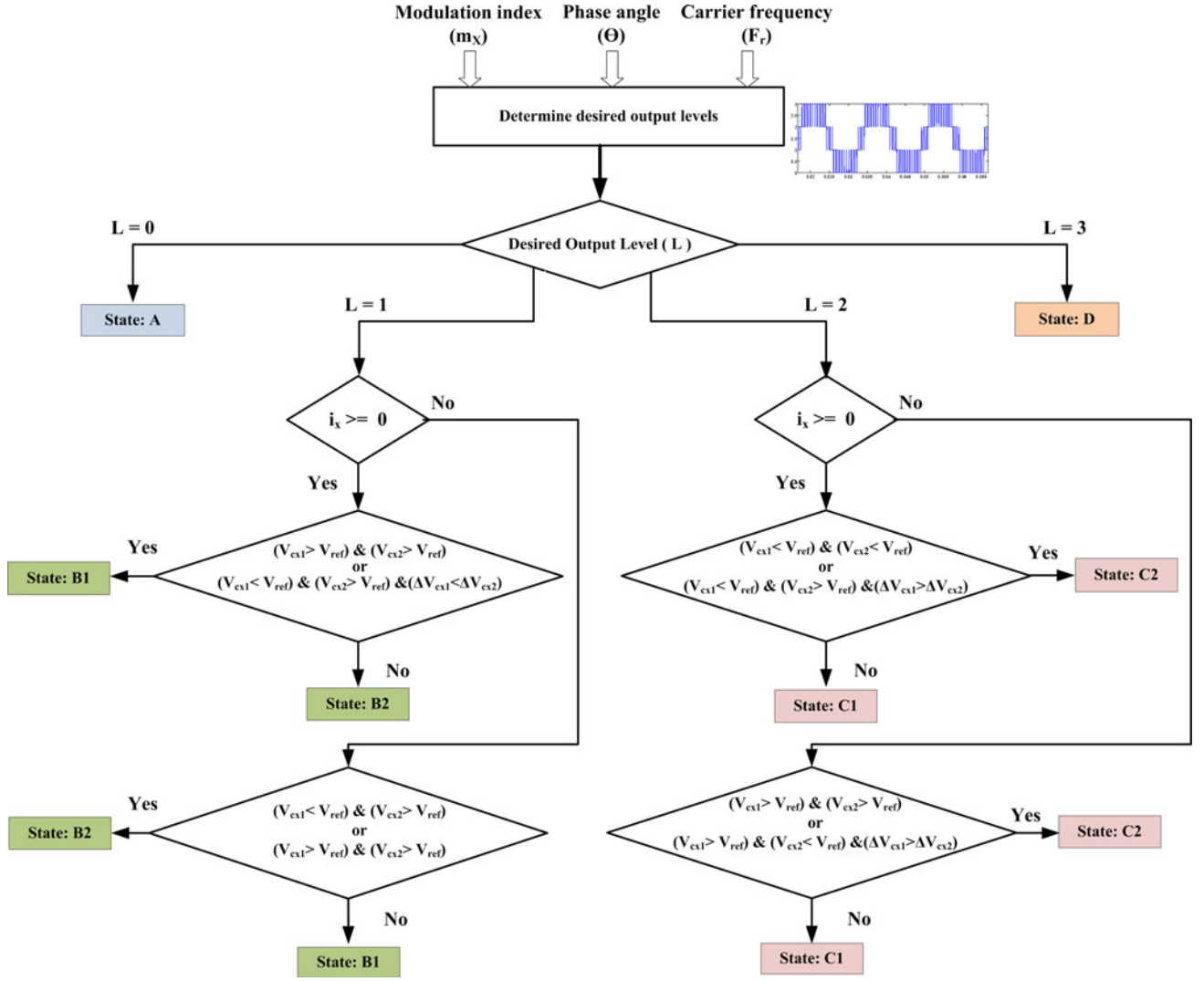


Fig. 6. Procedure of the proposed SPWM approach for phase x ($x = a, b, c$).

level $1/6V_{dc}$ and $-1/6V_{dc}$, there are two redundant switching states. Each redundant state provides a specific charging and discharging current path for each floating capacitor. This is a specific feature of redundant switching states that can be applied to achieve voltage balancing of the FCs. The main technical challenge is to identify the best switching state.

B. SVM Technique for the NNPC Converter

The SVM technique can be applied to the converter to control the output voltage and keep the capacitor voltages balanced and constant [16]. The space vector diagram of a four-level converter on the $\alpha - \beta$ plane is a hexagon centered at the origin of the plane, as shown in Fig. 3. The reference vector is synthesized by the three adjacent switching vectors and the can be describes as

$$\begin{aligned} \vec{V}_1 t_1 + \vec{V}_2 t_2 + \vec{V}_3 t_3 &= \vec{V}_{ref} T_s \\ t_1 + t_2 + t_3 &= T_s \\ \vec{V}_{ref} &= |\vec{V}_{ref}| e^{j\theta}, \quad \theta = \angle \vec{V}_{ref} \end{aligned} \quad (1)$$

where T_s is the switching period, \vec{V}_1 , \vec{V}_2 , and \vec{V}_3 are the three switching vectors adjacent to \vec{V}_{ref} and t_1 , t_2 , and t_3 are the calculated on-duration time intervals of the switching vectors, respectively. A cost function, J , can be defined based on the energy stored in the capacitors as follows:

$$\begin{aligned} J &= J_a + J_b + J_c \\ &= \sum_x \sum_{i=1}^2 \frac{1}{2} C_{cxi} \left(V_{cxi} - V_{Dc/3} \right)^2 \\ x &= a, b, c. \end{aligned} \quad (2)$$

The SVM approach has the following steps to generate three-phase output voltages and regulate FCs [16]:

- 1) identify the sector and triangle where reference vector is located in the $\alpha - \beta$ coordinate system;
- 2) determine the adjacent switching vectors;
- 3) duty-cycle calculation;
- 4) determine of redundant switching state combinations;

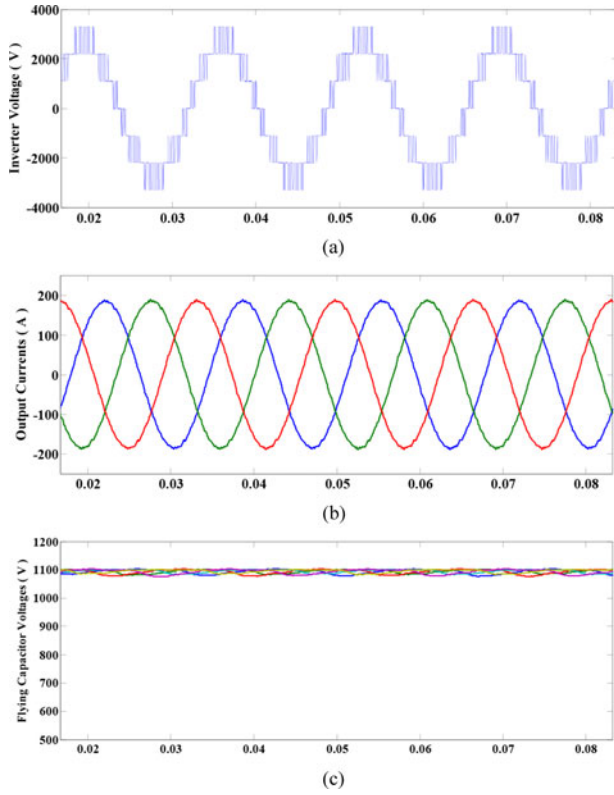


Fig. 7. Simulation waveforms with $m = 0.95$ (a) Inverter output voltage (b) Output currents (c) Voltage of flying capacitors.

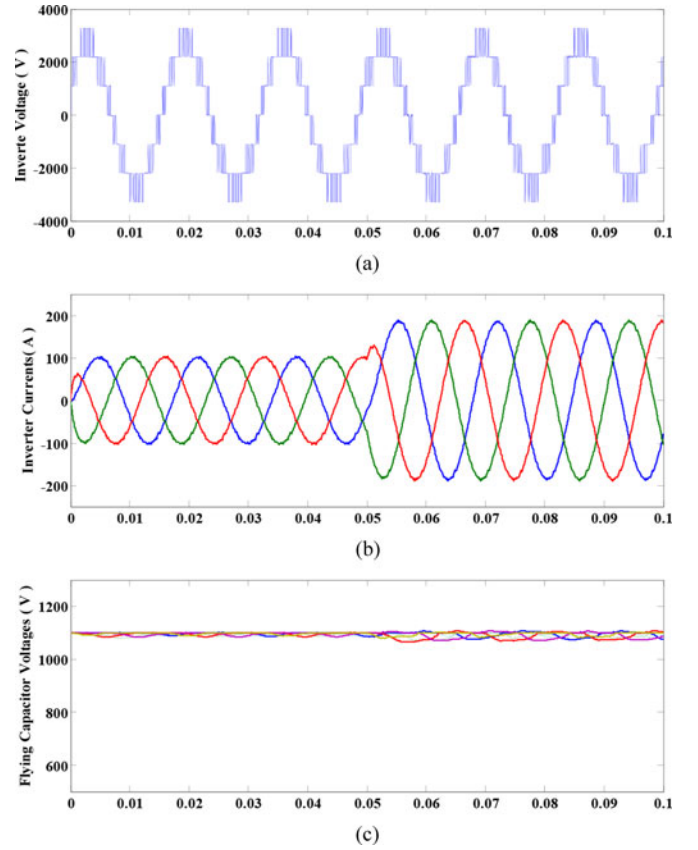


Fig. 9. Simulation waveforms; step change from half load to full load (a) Inverter Output voltages (b) Output currents (b) Voltage of flying capacitors.

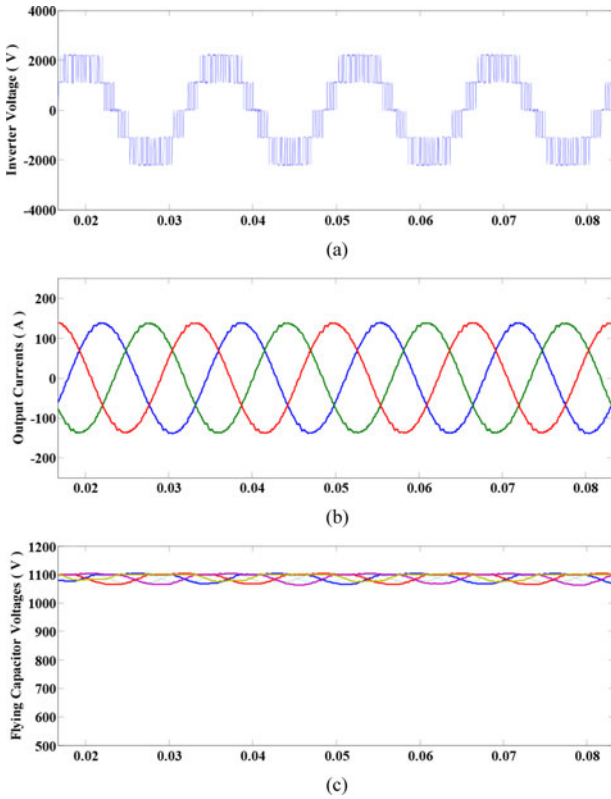


Fig. 8. Simulation waveforms with $m = 0.7$ (a) Inverter output voltage (b) Output currents (c) Voltage of flying capacitors.

- 5) calculate the average capacitor currents;
- 6) select the best switching states based on the minimization of energy property of the FCs.

This procedure can produce output voltages and regulate FCs; however, it has lots of calculations, which increases the complexity of the implementation and also introduces a considerable time delay in the actuation. This computational delay can deteriorate the performance of the control system. In order to reduce the complexity of the implementation, and thus, improve the performance of the whole system, a new simple PWM technique presented in Section III.

III. NEW AND SIMPLE SINGLE-PHASE MODULATOR FOR THE NNPC CONVERTER

The proposed single-phase modulator is based on an SPWM technique, which is described in Section I. This technique uses three-level-shifted triangular carriers, all having the same frequency and the same amplitude. The in-phase disposition method, where all carriers are in phase, has been employed for the four-level NNPC converter as shown in Fig. 4.

Comparing carriers and modulation signal, the desired output levels can be obtained, as shown in Fig. 5. Based on the desired level at the output, the corresponding switching state can be

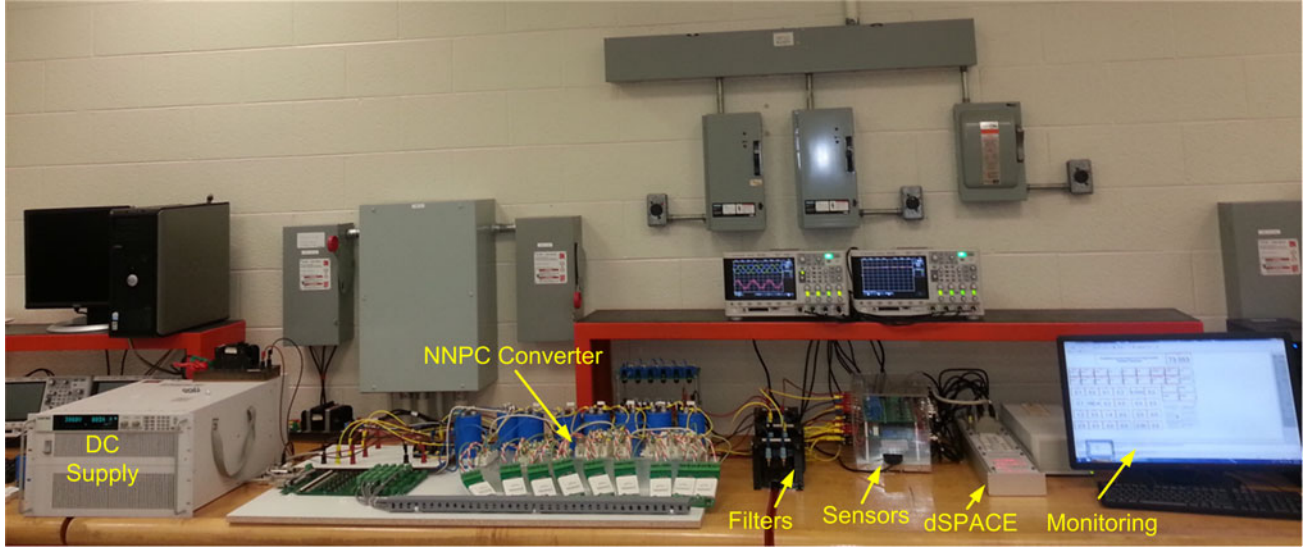


Fig. 10. Experimental setup for the NNPC converter.

selected from Table I, and then, applied to the power switches. Table I also shows that there are redundancy states for two middle levels (level 1 and 2). The redundancy states based on the direction of the output current can charge or discharge the FCs.

Therefore, after determining the desired output level (by comparing carriers and modulation signal), the direction of the phase current should be measured, and then, the controller will decide which states should be chosen to apply to the converter to control and balance the voltages of capacitors.

The selected switching state can charge or discharge the FCs to minimize the difference between the nominal voltage values and the measured voltage values. The diagram shown in Fig. 6 shows the procedure of the proposed SPWM approach. As can be seen from Fig. 5, this procedure is very simple and easy to implement in hardware in compare to the huge amount of calculations for the SVM technique. In the proposed approach, the amount of calculation is independent from the modulation index. The main feature of the proposed SPWM technique is that it can be applied to each leg separately to control the FCs of that leg and at the same time, generate output waveforms. In different phases, just the modulating signals have $\pm 120^\circ$ phase shift respect to each other.

IV. SIMULATION RESULTS

In order to show the performance of the proposed SPWM approach for the NNPC converter, simulation studies have been done in MATLAB/Simulink environment. The simulation studies demonstrate the effectiveness of the developed SPWM to generate output voltages and regulate the voltage of FCs. The parameters used in simulation studies can be found in Table II. The performance of the proposed SPWM controller has been studied during steady state and transient state.

TABLE II
PARAMETERS OF THE STUDY SYSTEM (SIMULATION)

Converter Parameters	Values
Converter Rating	0.5 MVA
FCs	2200 μ F
Input DC Voltage	3.3 kV
Output Frequency	60 Hz
Output Inductance	5 mH
Output Load	7.5 Ω

A. Steady-State Analysis

Figs. 7 and 8 show the performance of the NNPC converter using an SPWM technique with different modulation indexes. Fig. 7 shows the inverter output voltage, output currents, and FC voltages where modulation index $m = 0.95$. Fig. 8 also shows the inverter output voltage, output currents, and FC voltages where modulation index $m = 0.7$.

As can be seen from the Figs. 7 and 8, the proposed SPWM technique can regulate and balance the capacitor voltages under various different conditions.

B. Transient-State Analysis

To evaluate the dynamic performance of the proposed SPWM controller, a load step-change has been studied. In this case, a step change from half load to full load ($m = 0.95$) is applied to the system. Fig. 9 shows the performance of the controller that can maintain the voltages of FCs at the nominal values.

V. EXPERIMENTAL RESULTS

The feasibility of the proposed SPWM technique is evaluated experimentally. The parameters shown in Table III were used to obtain experimental results from a scaled-down prototype. The

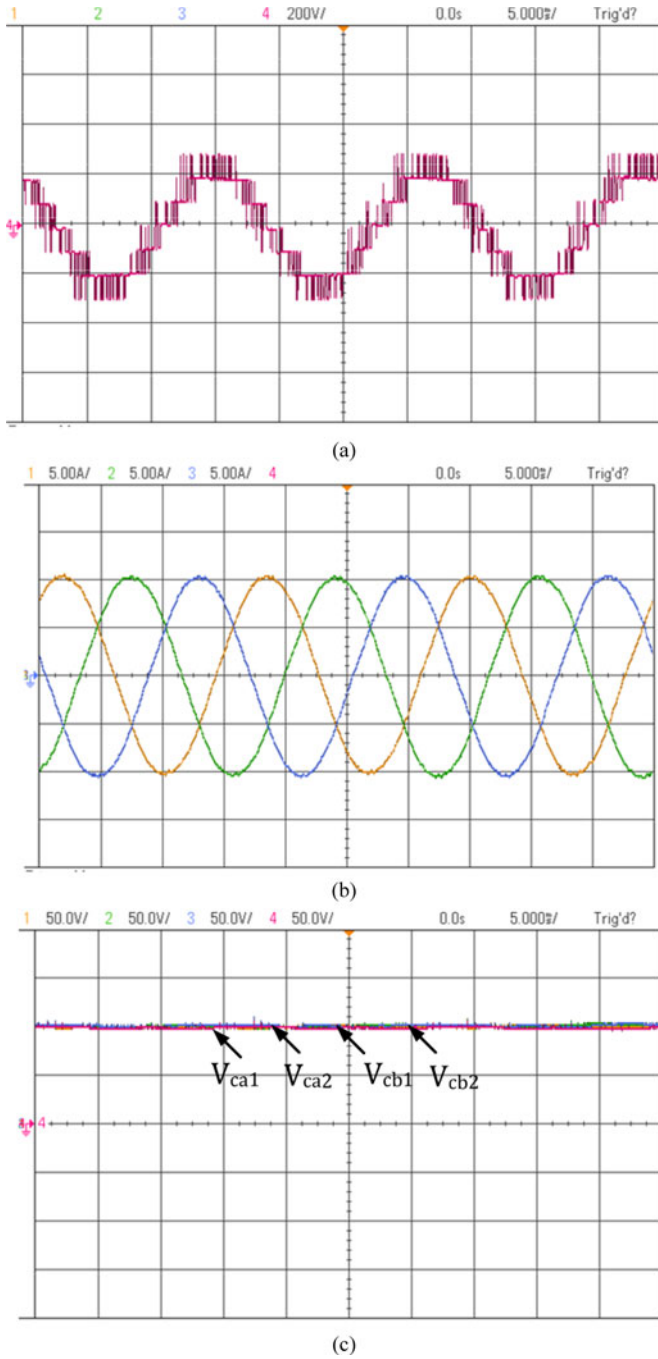


Fig. 11. Experimental waveforms for NNPC converter, $m = 0.95$. (a) Inverter voltage, (b) inverter output currents, (c) voltage of FCs.

TABLE III
PARAMETERS OF THE STUDY SYSTEM (EXPERIMENTAL)

Converter Parameters	Values
Converter Rating	5 kVA
FCs	1000 μ F
Input DC Voltage	300 V
Output Frequency	60 Hz
Output Inductance	5 mH
Output Load	10 Ω

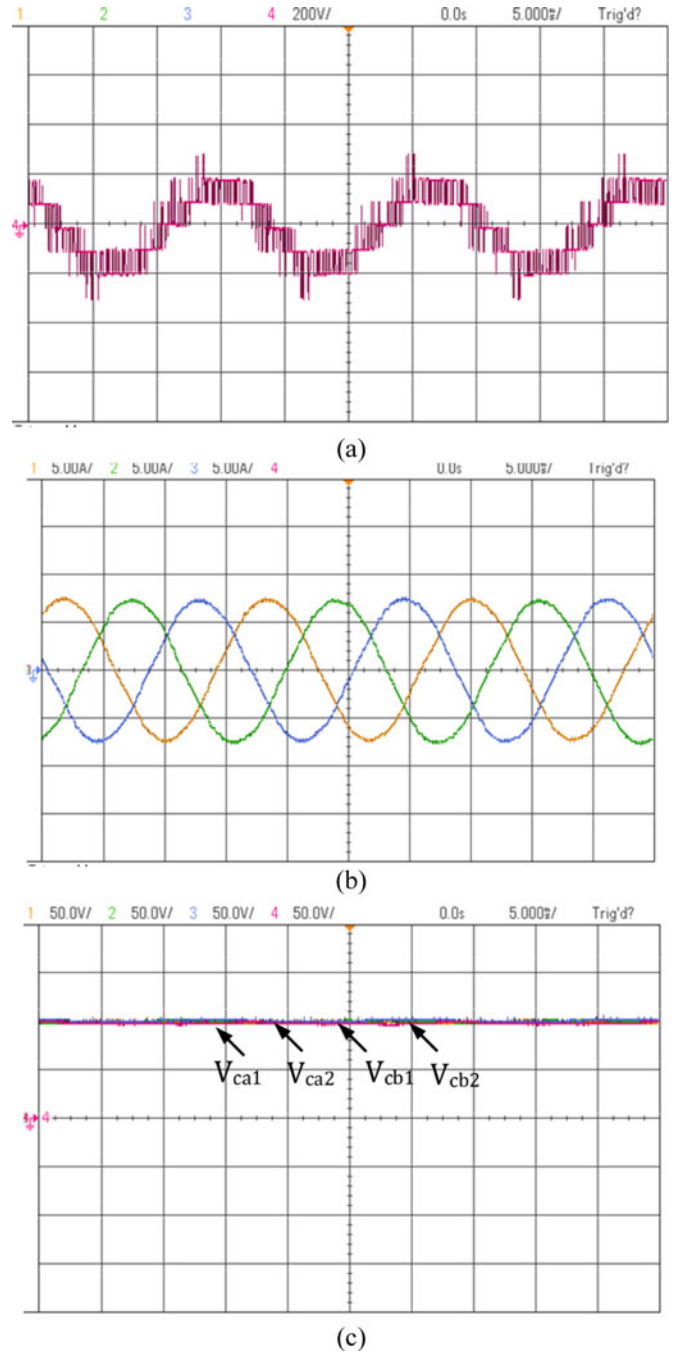


Fig. 12. Experimental waveforms for the NNPC converter, $m = 0.7$. (a) Inverter voltage, (b) inverter output currents (c) voltage of FCs.

experimental setup for the four-level NNPC converter is shown in Fig. 10.

The proposed modulation scheme was implemented using a PC with MATLAB-Simulink. The real-time controller was the dSPACE DS1103 controller. The load currents and FC voltages were measured by LEM LA 100-P and LV 25-P transducers, respectively. The feedbacks from the sensors were sent to the DS1103 through I/O connector. Table IV shows the devices were used to implement the scaled-down prototype.

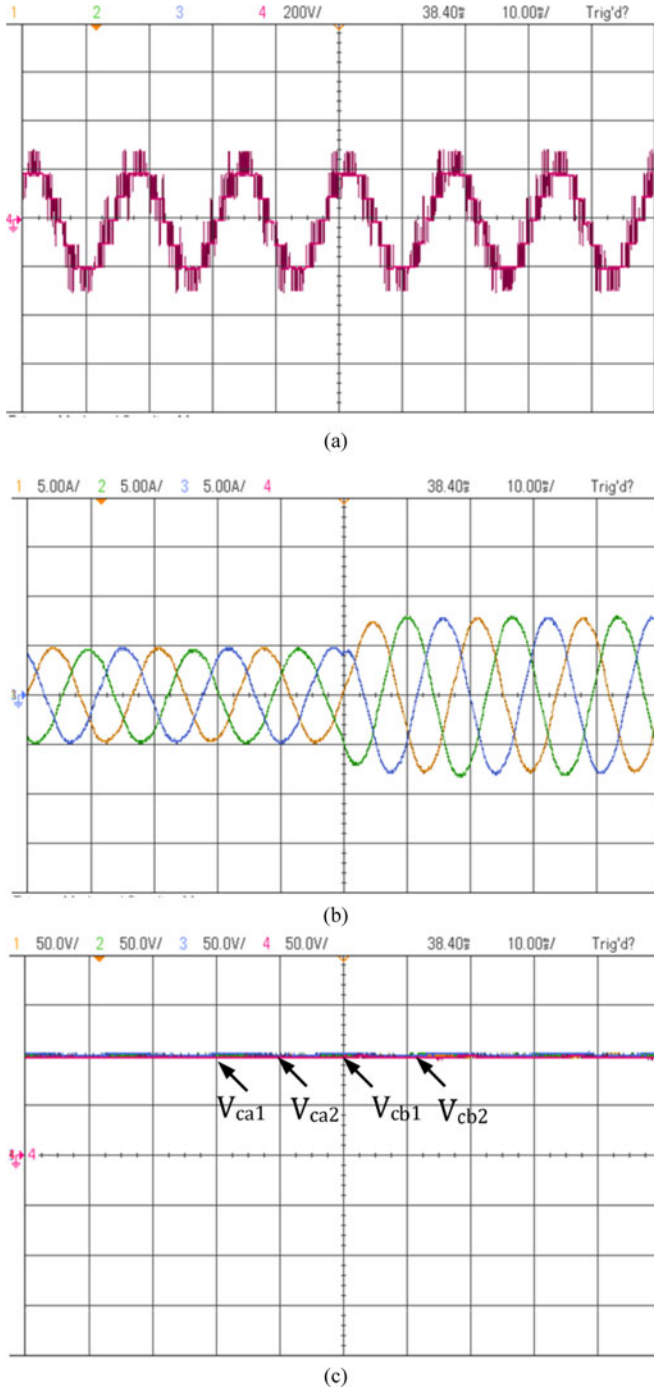


Fig. 13. Experimental waveforms for the NNPC converter, ($m = 0.95$). Step change from half load to full load. (a) Inverter voltage, (b) inverter output currents (c) voltage of FCs.

TABLE IV
COMPONENTS OF THE PROTOTYPE CONVERTER

Converter Parameters	Values
Power Switches	IGBT SKM75GB123D
Gate Drivers	SKH122B
Power Diodes	SKKD75F12
DC Power Supply	Xantrex XDC-600-20

The gating signals were sent to the SKH122B gate drivers through an interface board consisting of MC14504BCP and TLP521-4 for TTL to CMOS logic conversion and isolation.

Figs. 11 and 12 show the performance of the proposed converter under different operating conditions. Fig. 11 shows the inverter output voltage, output currents, and FC voltages where modulation index $m = 0.95$. Fig. 12 also shows the inverter output voltage, output currents, and FC voltages where modulation index $m = 0.7$.

Fig. 13 shows the performance of the proposed converter under transient condition when load changes from half load to full load. As can be seen from Figs. 11 to 13, in all cases, capacitor voltages are well balanced.

VI. CONCLUSION

This paper introduces a new SPWM technique for an NNPC converter. The NNPC converter that is a four-level converter topology for medium-voltage applications has interesting properties; operating over a wide range of voltages, high quality output voltage, and less number of components in compare to other classical four-level topologies. This paper presents a simple single-phase modulator that can be applied to each phase of a three-phase NNPC converter and for different phases, the modulating signals have $\pm 120^\circ$ phase shift respect to each other. The proposed technique employs the redundant switching states and selects the best switching state based on the direction of the output current to regulate voltage of FCs to their desired values. Performance of the proposed technique under different operating conditions was investigated in the MATLAB/Simulink environment. The feasibility of the proposed converter was evaluated experimentally.

REFERENCES

- [1] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.
- [2] B. Wu, *High-Power Converters and AC Drives*. Piscataway, NJ, USA: IEEE Press, 2006.
- [3] J. Rodriguez, J. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
- [4] J. Rodriguez, S. Bernet, B. Wu, J. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.
- [5] M. Saeedifard, P. M. Barbosa, and P. K. Steimer, "Operation and control of a hybrid seven-level converter," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 652–660, Feb. 2012.
- [6] Z. Cheng and B. Wu, "A novel switching sequence design for five-level NPC/H-bridge inverters with improved output voltage spectrum and minimized device switching frequency," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2138–2145, Nov. 2007.
- [7] I. Etxeberria-Otadui, A. L. de Heredia, J. San-Sebastian, H. Gaztaaga, U. Viscarret, and M. Caballero, "Analysis of a H-NPC topology for an AC traction front-end converter," in *Proc. 13th Power Electron. Motion Control Conf.*, Sep. 1–3, 2008, pp. 1555–1561.
- [8] V. Guennegues, B. Gollentz, L. Leclerc, F. Meibody-Tabar, and S. Rael, "Selective harmonic elimination PWM applied to H-bridge topology in high speed applications," in *Proc. Int. Conf. POWERENG*, Mar. 18–20, 2009, pp. 152–156.
- [9] C. M. Wu, W. H. Lau, and H. Chung, "A five-level neutral-point-clamped H-bridge PWM inverter with superior harmonics suppression: A

- theoretical analysis," in *Proc. IEEE Int. Symp. Circuits Syst.*, Orlando, FL, USA, May 30–Jun. 2, 1999, vol. 5, pp. 198–201.
- [10] T. Bruckner, S. Bernet, and H. Guldner, "The active NPC converter and its loss-balancing control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 855–868, Jun. 2005.
 - [11] O. Apeldoorn, B. Odegard, P. Steimer, and S. Bernet, "A 16 MVA ANPC-PEBB with 6 ka IGBTs," in *Proc. Conf. Rec. 40th IEEE IAS Annu. Meeting*, Oct. 2–6, 2005, vol. 2, pp. 818–824.
 - [12] J. Meili, S. Ponnaluri, L. Serpa, P. K. Steimer, and J. W. Kolar, "Optimized pulse patterns for the 5-level ANPC converter for high speed high power applications," in *Proc. 32nd IEEE Ind. Electron. Conf.*, Nov. 6–10, 2006, pp. 2587–2592.
 - [13] L. A. Serpa, P. M. Barbosa, P. K. Steimer, and J. W. Kolar, "Fivelevel virtual-flux direct power control for the active neutral-point clamped multilevel inverter," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 15–19, 2008, pp. 1668–1674.
 - [14] F. Kieferndorf, M. Basler, L. A. Serpa, J.-H. Fabian, A. Coccia, and G. A. Scheuer, "A new medium voltage drive system based on anpc-5l technology," in *Proc. IEEE-Int. Conf. Ind. Technol.*, Viña del Mar, Chile, Mar. 2010, pp. 605–611.
 - [15] P. Barbosa, P. Steimer, J. Steinke, L. Meysenc, M. Winkelkemper, and N. Celanovic, "Active neutral-point-clamped multilevel converters," in *Proc. IEEE 36th Power Electron. Spec. Conf.*, Jun. 16, 2005, pp. 2296–2301.
 - [16] M. Narimani, B. Wu, G. Cheng, and N. Zargari, "A New nested neutral point clamped (NNPC) converter for medium-voltage (MV) power conversion," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6375–5382, Dec. 2014.
 - [17] K. Hasegawa and H. Akagi, "A new dc-balancing circuit including a single coupled inductor for a five-level diode-clamped PWM converter," *IEEE Trans. Ind. Appl.*, vol. 47, no. 2, pp. 841–852, Mar./Apr. 2011.
 - [18] Z. Pan, F. Z. Peng, K. A. Corzine, V. R. Stefanovic, J. M. Leuthen, and S. Gataric, "Voltage balancing control of diode-clamped multilevel rectifier/inverter systems," *IEEE Trans. Ind. Appl.*, vol. 41, no. 6, pp. 1698–1706, Nov./Dec. 2005.
 - [19] K. Kaneko, M. Jun, S. Kiyooki, K. Matsuse, A. Yasushi, and H. Lipei, "Analysis of dynamic variation on a combined control strategy for a five-level double converter," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2005, pp. 885–891.
 - [20] Y. Cheng, C. Qian, M. L. Crow, S. Pekarek, and S. Atcitty, "A comparison of diode-clamped and cascaded multilevel converters for a STATCOM with energy storage," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1512–1521, Oct. 2006.
 - [21] H. Akagi, H. Fujita, S. Yonetani, and Y. Kondo, "A 6.6-kV transformerless STATCOM based on a five-level diode-clamped PWM converter: System design and experimentation of a 200-V, 10-kVA laboratory model," in *Proc. IEEE 40th Ind. Appl. Soc. Annu. Meeting*, Oct. 2005, vol. 1, pp. 557–564.
 - [22] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 637–641, Mar./Apr. 2001.
 - [23] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, Aug. 2002.
 - [24] R. S. Kanchan, K. Gopakumar, and R. Kennel, "Synchronised carrier based SVPWM signal generation scheme for the entire modulation range extending up to six-step mode using the sampled amplitudes of reference phase voltages," *IET Elect. Power Appl.*, vol. 1, no. 3, pp. 407–415, May 2007.
 - [25] O. Lopez, J. Alvarez, J. Doval-Gandoy, and F. D. Freijedo, "Multilevel multiphase space vector PWM algorithm," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 1933–1942, May 2008.
 - [26] M. A. S. Aneesh, A. Gopinath, and M. R. Baiju, "A simple space vector PWM generation scheme for any general n -level inverter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1649–1656, May 2009.
 - [27] A. Shukla, A. Ghosh, and A. Joshi, "Hysteresis modulation of multilevel inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1396–1409, May 2011.
 - [28] Z. Zhao, Y. Zhong, H. Gao, L. Yuan, and T. Lu, "Hybrid selective harmonic elimination PWM for common-mode voltage reduction in three-level neutral-point-clamped inverters for variable speed induction drives," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1152–1158, Mar. 2012.
 - [29] J. Pou, J. Zaragoza, S. Ceballos, M. Saeedifard, and D. Boroyevich, "A carrier-based PWM strategy with zero-sequence voltage injection for a three-level neutral-point-clamped converter," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 642–651, Feb. 2012.
 - [30] J. Shen, S. Schroder, R. Rosner, and S. El-Barbary, "A comprehensive study of neutral-point self-balancing effect in neutral-point-clamped three-level inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3084–3095, Nov. 2011.
 - [31] M. Saeedifard, R. Iravani, and J. Pou, "Analysis and control of DC-capacitor-voltage-drift phenomenon of a passive front-end five-level converter," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3255–3266, Dec. 2007.
 - [32] S. Choi and M. Saeedifard, "Capacitor voltage balancing of flying capacitor multilevel converters by space vector PWM," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1154–1161, Jul. 2012.
 - [33] Y. Deng, K. H. Teo, C. Duan, T. G. Habetler, and R. G. Harley, "A fast and generalized space vector modulation scheme for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5204–5217, Oct. 2014.
 - [34] B. P. McGrath, D. G. Holmes, and T. Lipo, "Optimized space vector switching sequences for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1293–1301, Nov. 2003.
 - [35] Z. Shu, N. Ding, J. Chen, H. Zhu, and X. He, "Multilevel SVPWM with DC-link capacitor voltage balancing control for diode-clamped multilevel converter based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1884–1896, May 2013.



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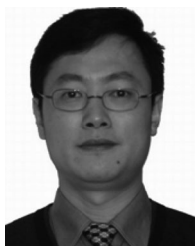
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